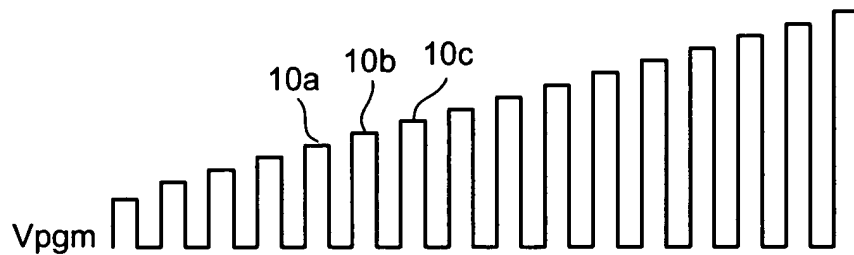


Fig. 1



of cells

Fig. 2

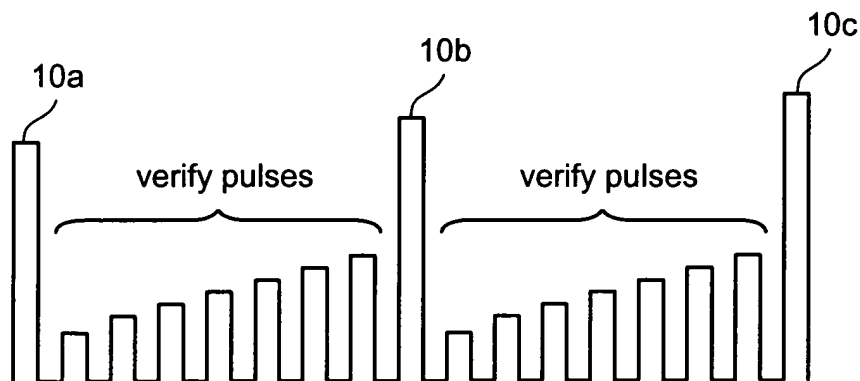
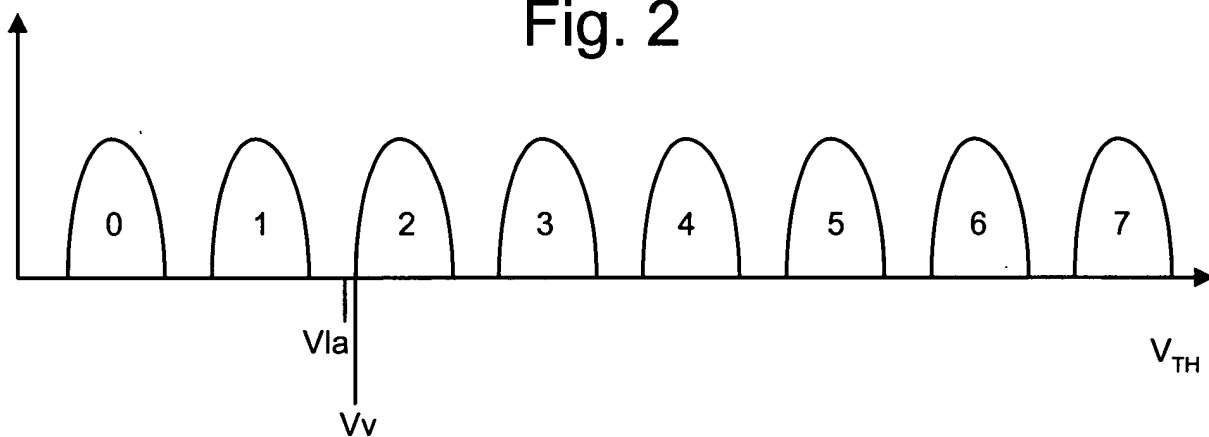


Fig. 3

Fig. 4

The diagram illustrates a memory system architecture with the following components and connections:

- Controller (27)**: Connected to a **Host (35)** via a bidirectional arrow. It has a **Control/Status** output (33) to the **Steering Gates** and a **Control/Status** input (31) from the **Select Gates**. It also has a **Bus** input (25) from the **Select Gates** and a **Control/Status** input (29) from the **Bit Line Decoder**.
- Steering Gates Decoders and Drivers (21)**: Receives **Control/Status** signals (33) from the Controller and has a bidirectional connection (23) with the **memory array**.
- Select Gates (Word Lines) Decoders and Drivers (19)**: Receives **Control/Status** signals (31) from the Controller and a **Bus** signal (25) from the **memory array**. It has a bidirectional connection (17) with the **memory array** and a **Control/Status** output (13) to the **Bit Line Decoder**.
- memory array (11)**: The central storage component, connected to the **Steering Gates** (23), **Select Gates** (17), and **Bit Line Decoder** (15).
- Bit Line Decoder, Drivers and Sense Amplifiers (22)**: Receives **Control/Status** signals (13) from the **Select Gates** and has a bidirectional connection (15) with the **memory array**. It outputs a **Read** signal (41) to the **Controller**.

[illegible]

This diagram shows a cross-sectional view of a memory array structure. It features three vertical access transistors labeled T1-Left, T2, and T1-Right. T1-Left and T1-Right are equipped with steering gates, labeled 'Left Steering Gate' and 'Right Steering Gate' respectively. A central 'Select Gate (Word Line)' is positioned above the T2 transistor. Bit lines are labeled 'BL left' (49') and 'BL right' (51'). Various other components and regions are labeled with reference numerals: 55', 81', 56', 57', 58', 83', 92', and 99'.

Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW (2) ERASE (TO WORD LINE) (3) READ LEFT FLOATING GATE (4) READ RIGHT FLOATING GATE (5) PROGRAM LEFT FLOATING GATE (6) PROGRAM RIGHT FLOATING GATE (7) NO PROGRAM IN SELECTED ROW	0 V_E V_{SR} V_{SR} V_{SP} V_{SP} V_{SP}	X 5 0 1 5 0 0 5	X 0 V_M V_{BR} V_P V_{BP} X X	X 0 V_{BR} V_M V_{BP} V_P X X	X 5 1 0 0 5 0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO V_E , AND THE SUBSTRATE AT ZERO VOLTS]	V_{SE}	FLOAT	0	0	FLOAT

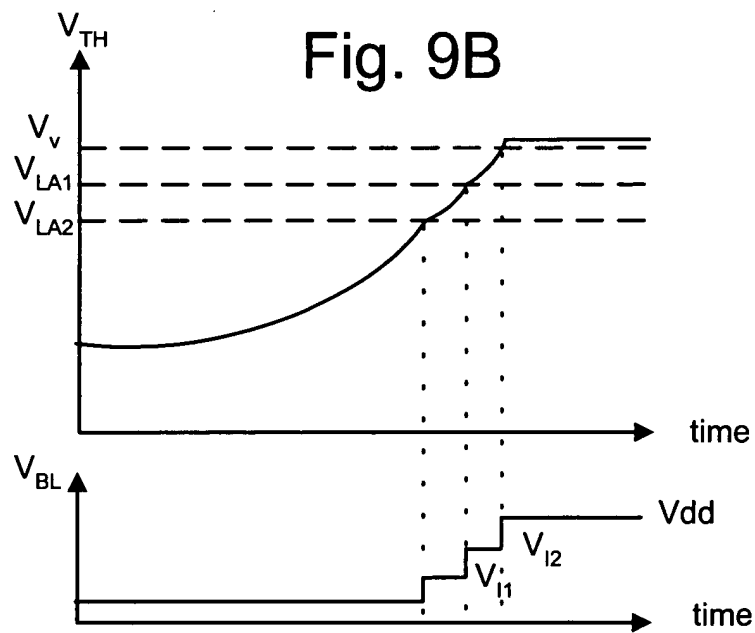
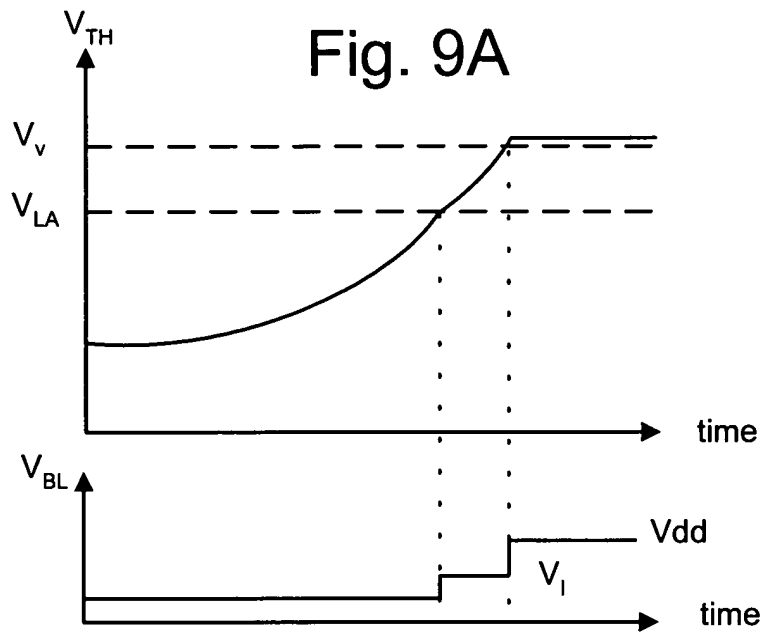
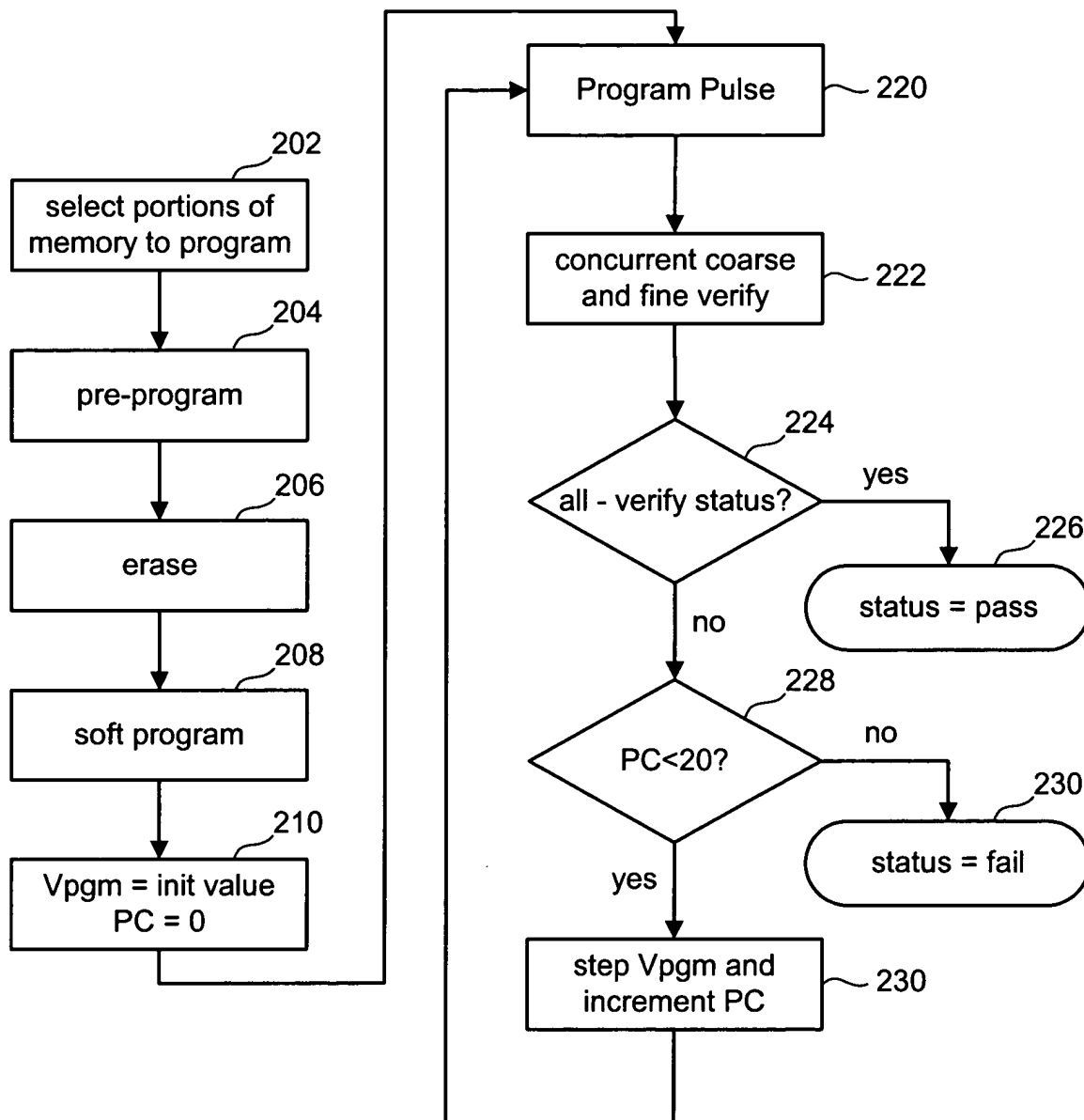


Fig. 10



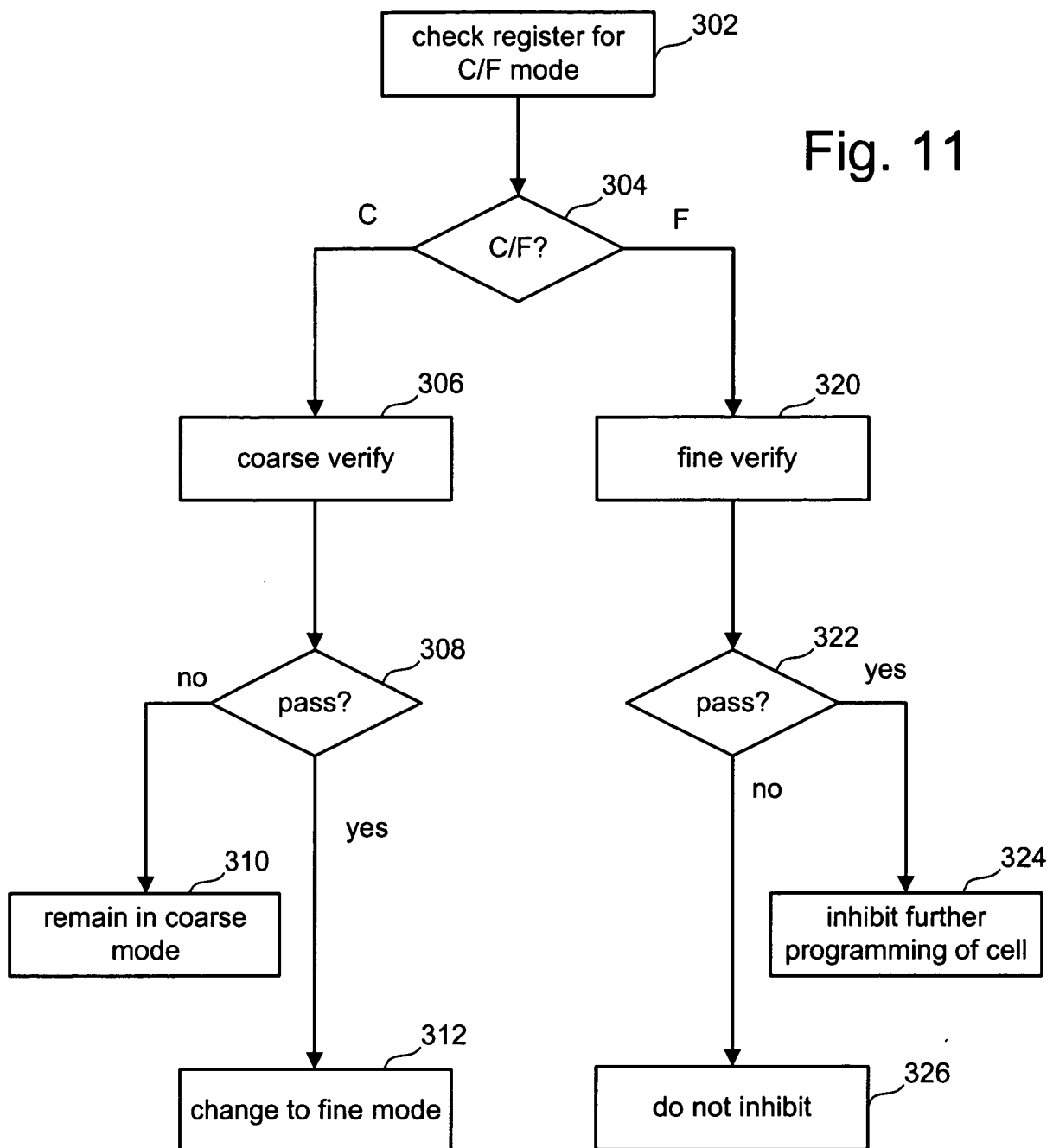


Fig. 12

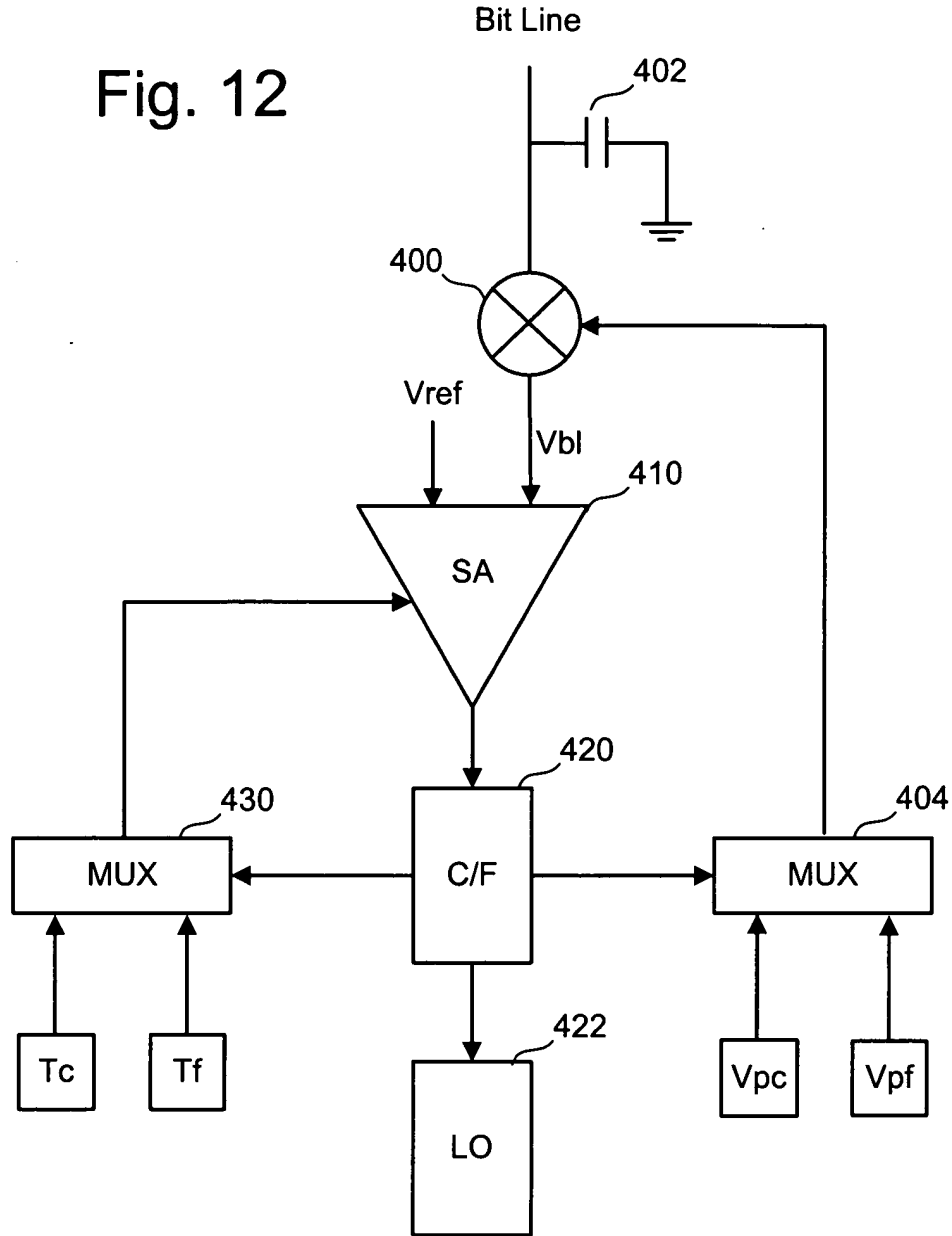


Fig. 13

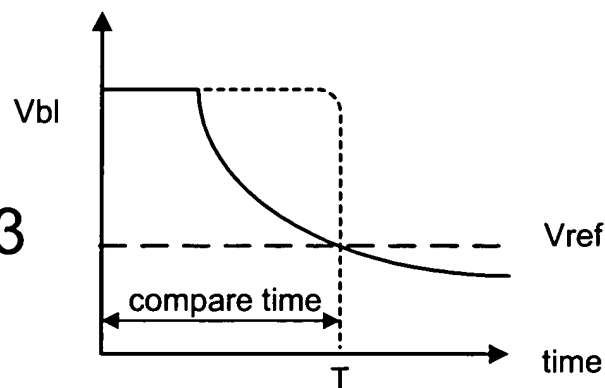


Fig. 14

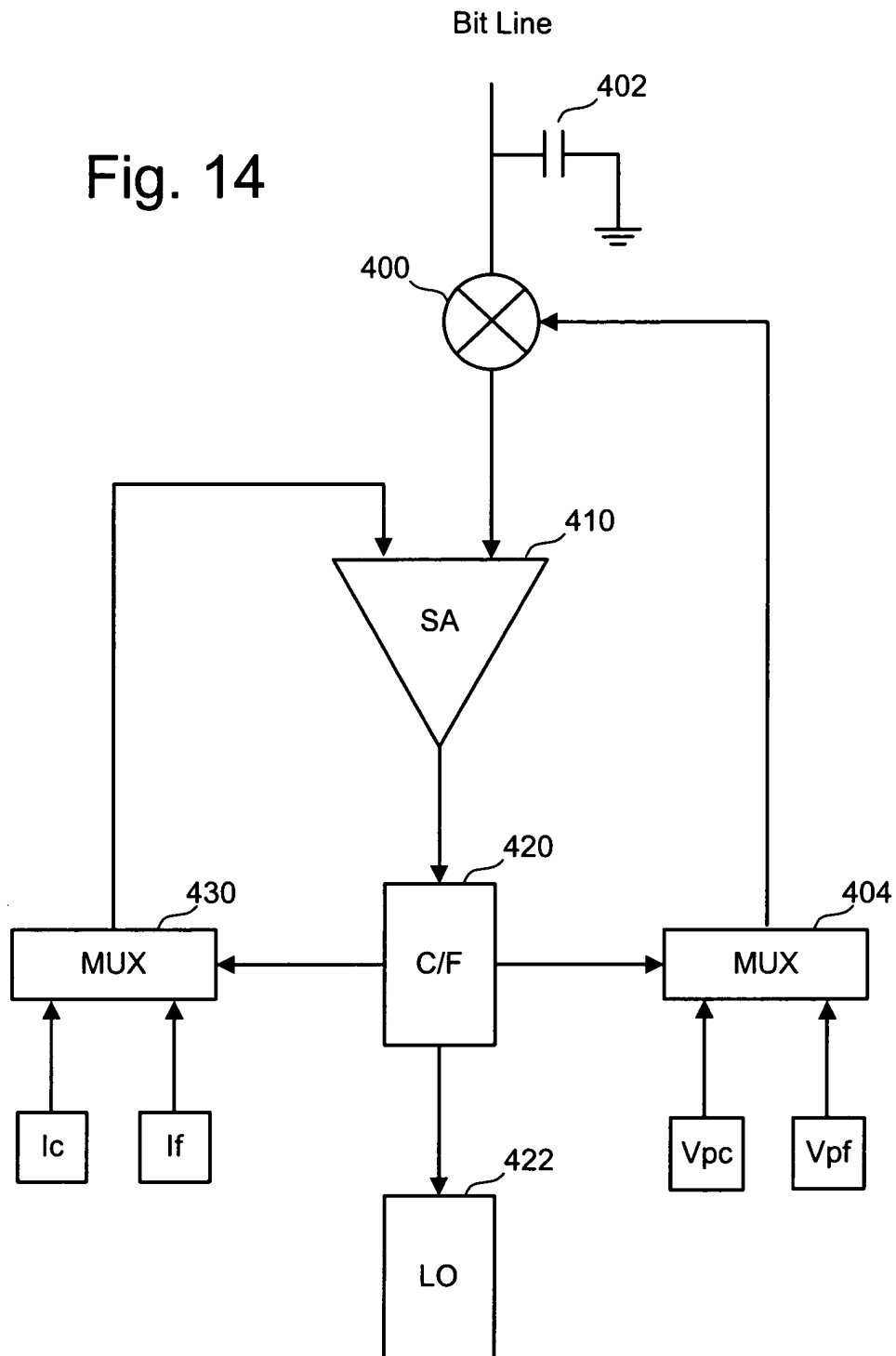


Fig. 15

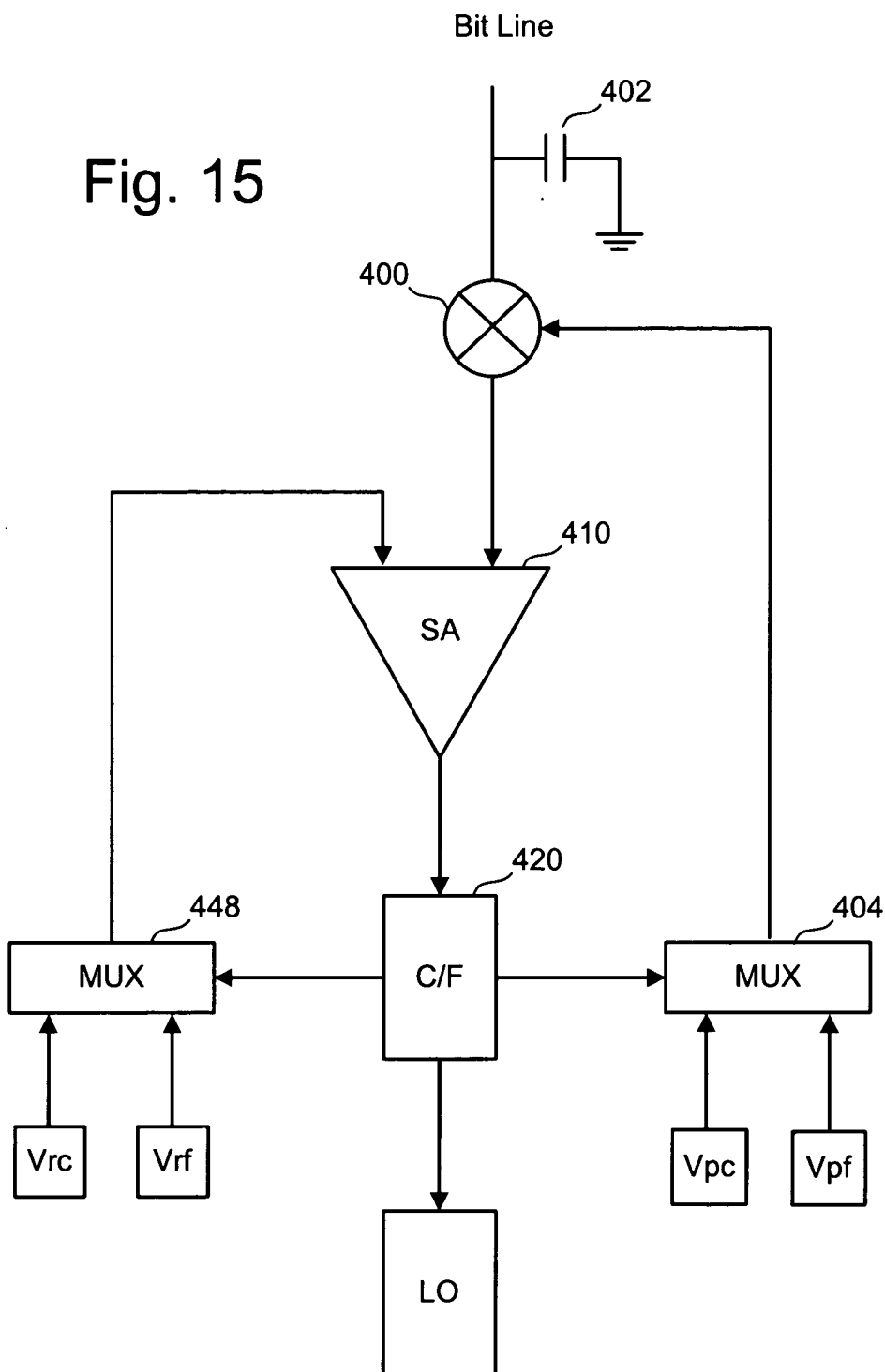


Fig. 16

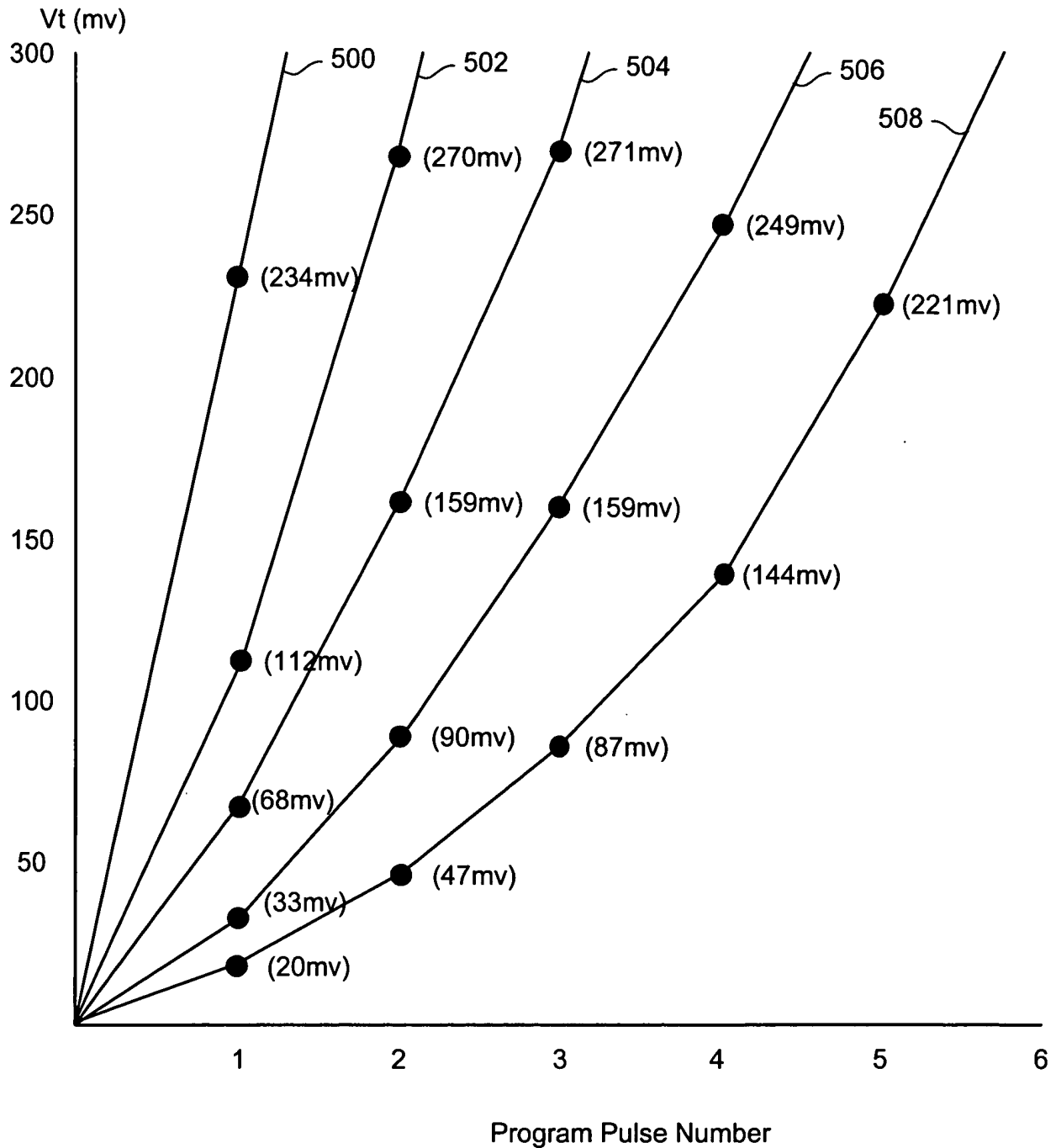


Fig. 17

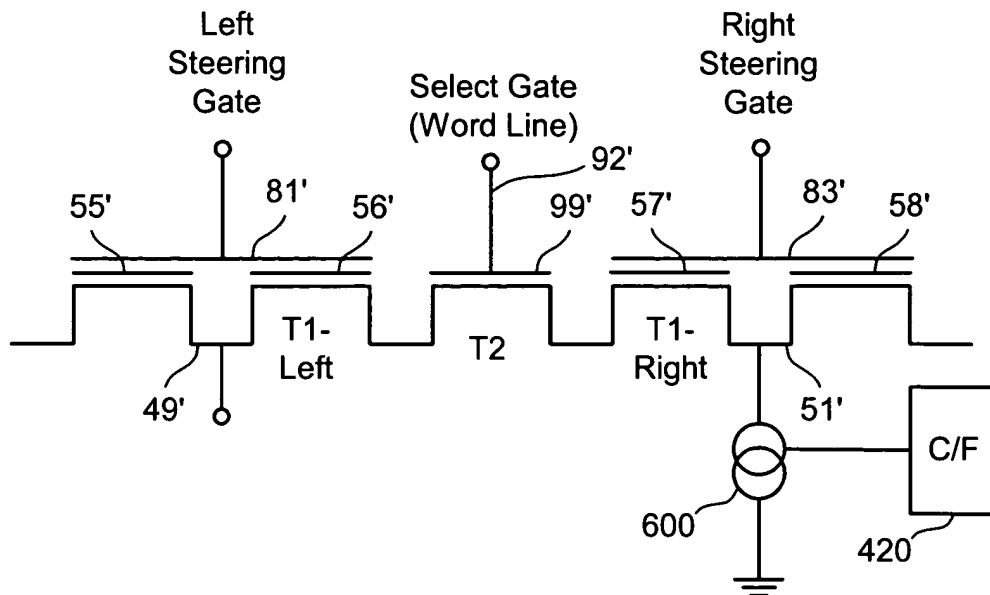


Fig. 18

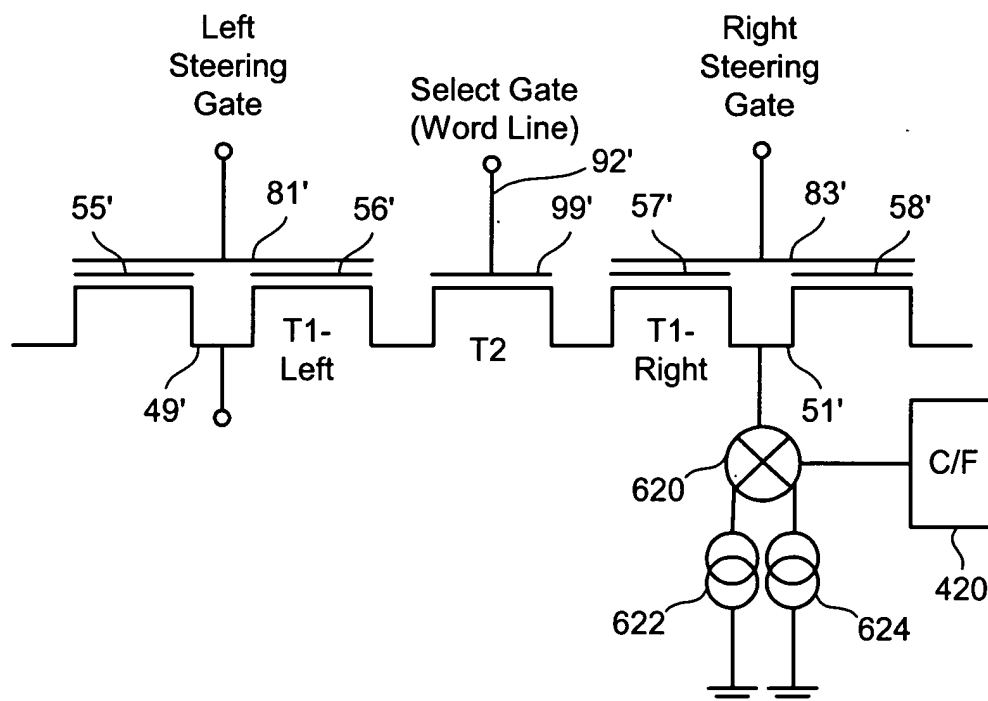
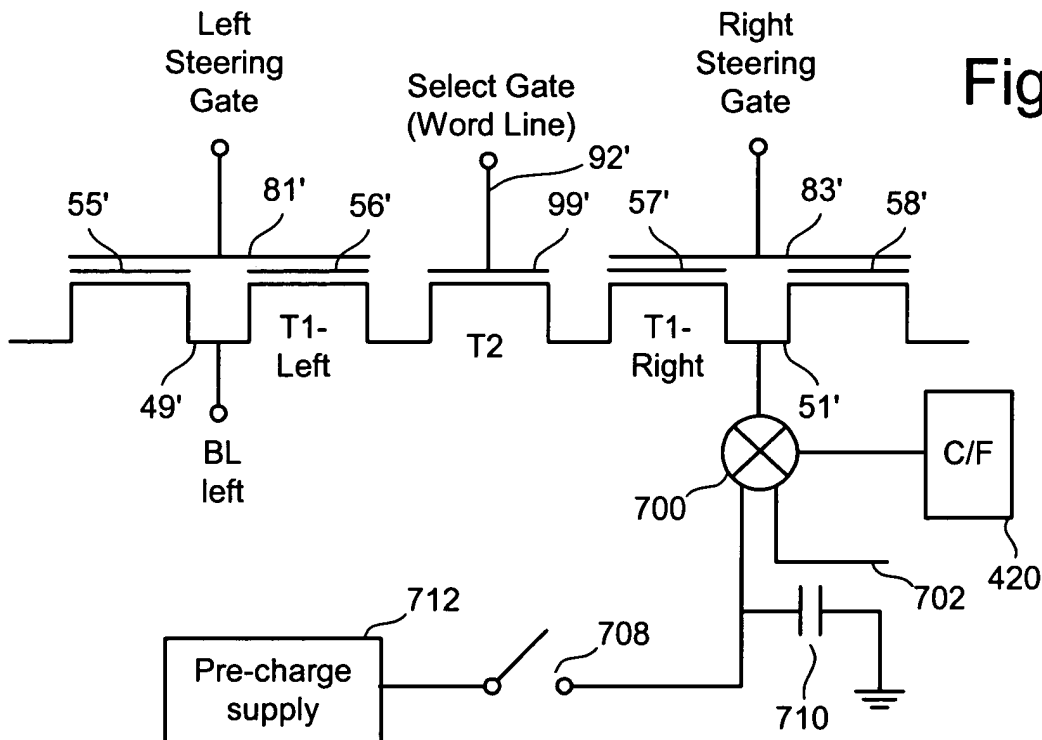
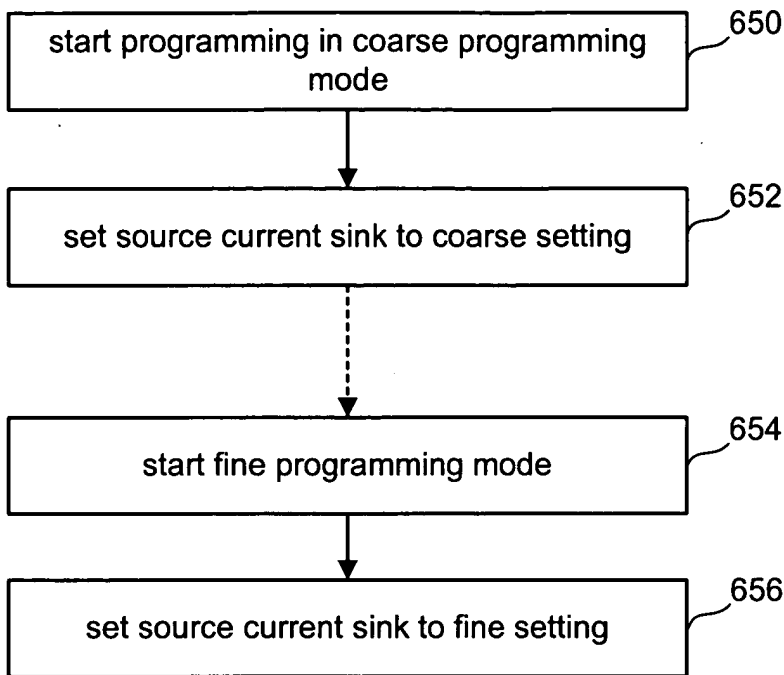


Fig. 19



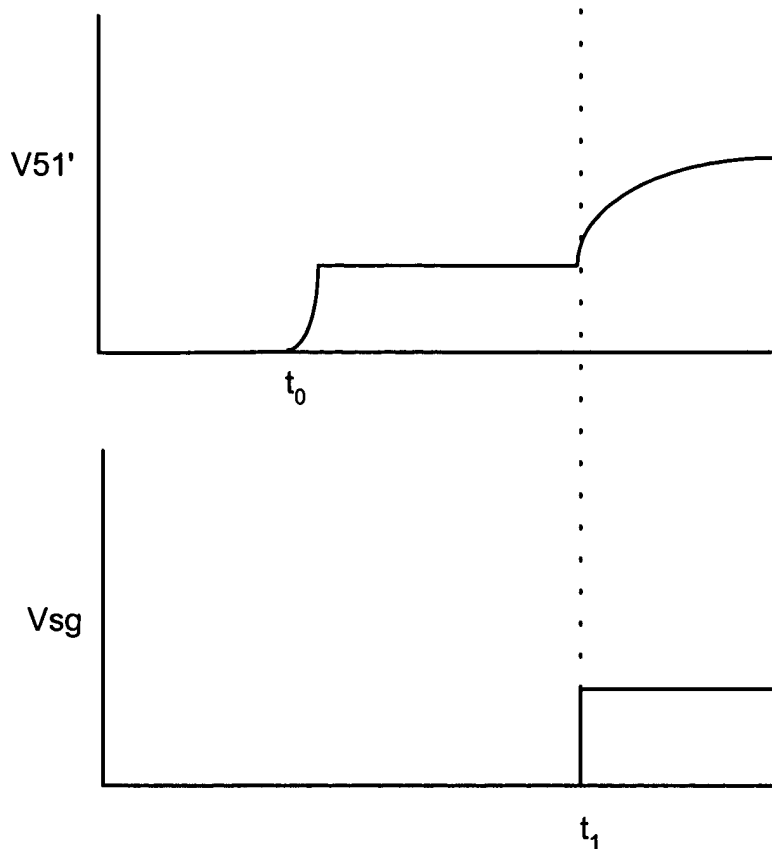


Fig. 21

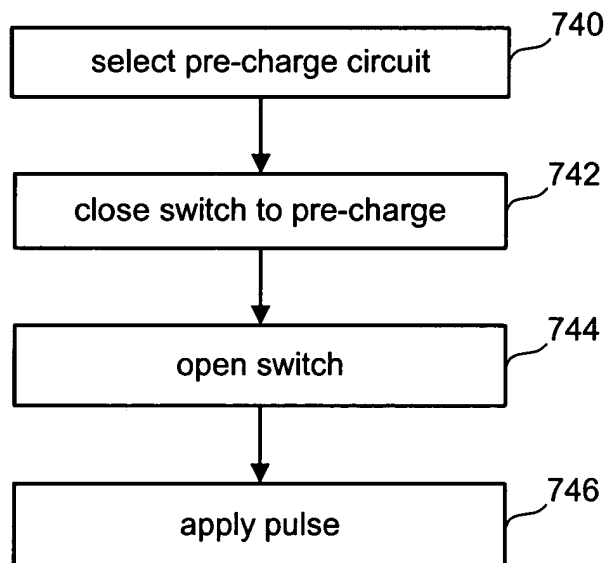


Fig. 22

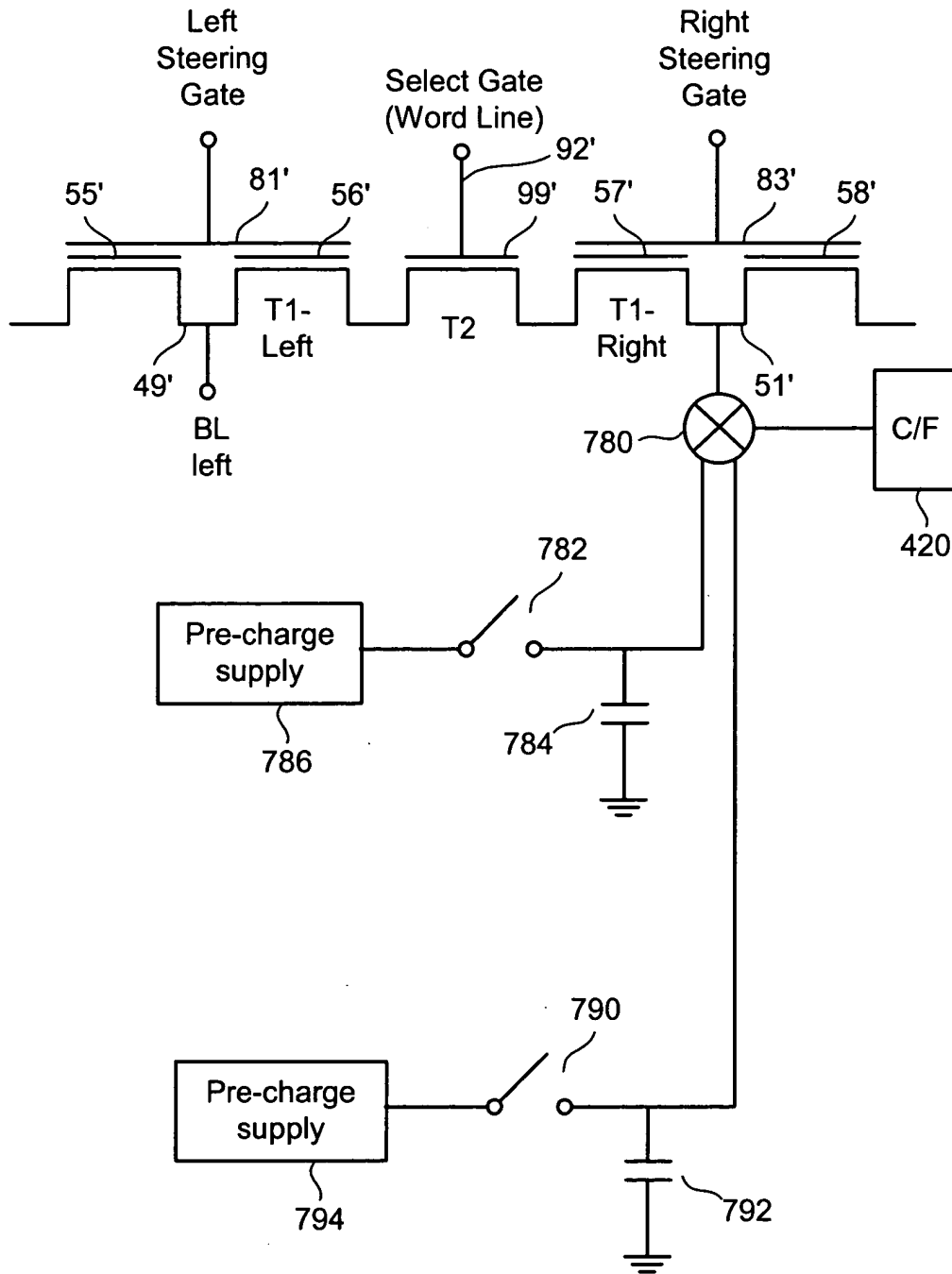


Fig. 23

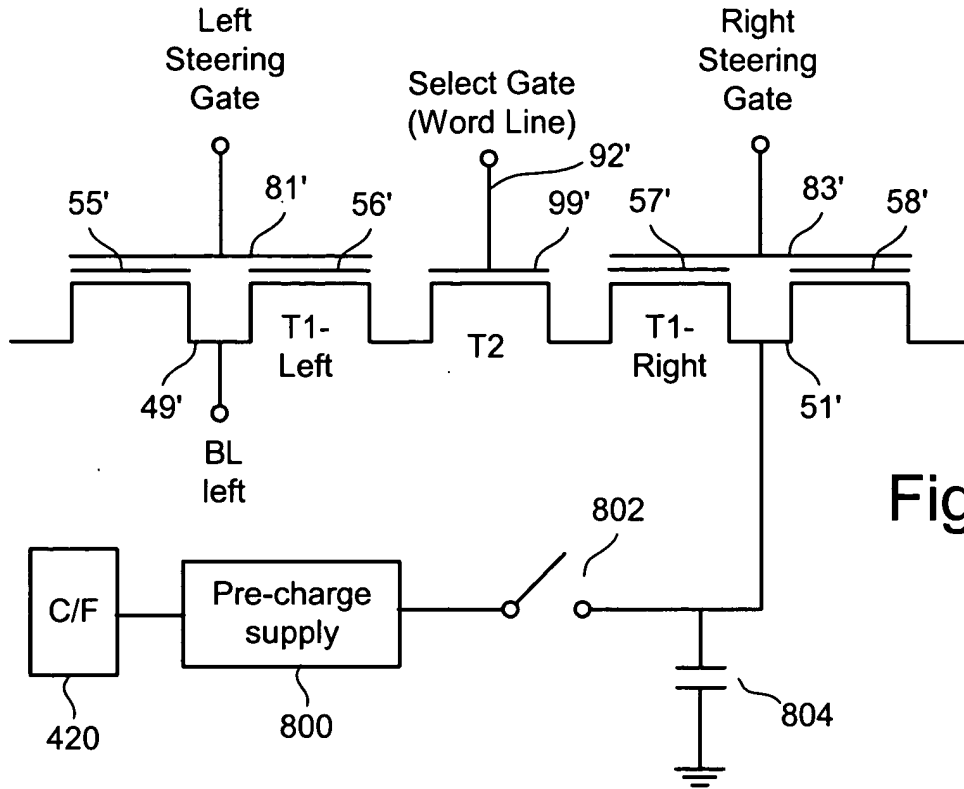


Fig. 24

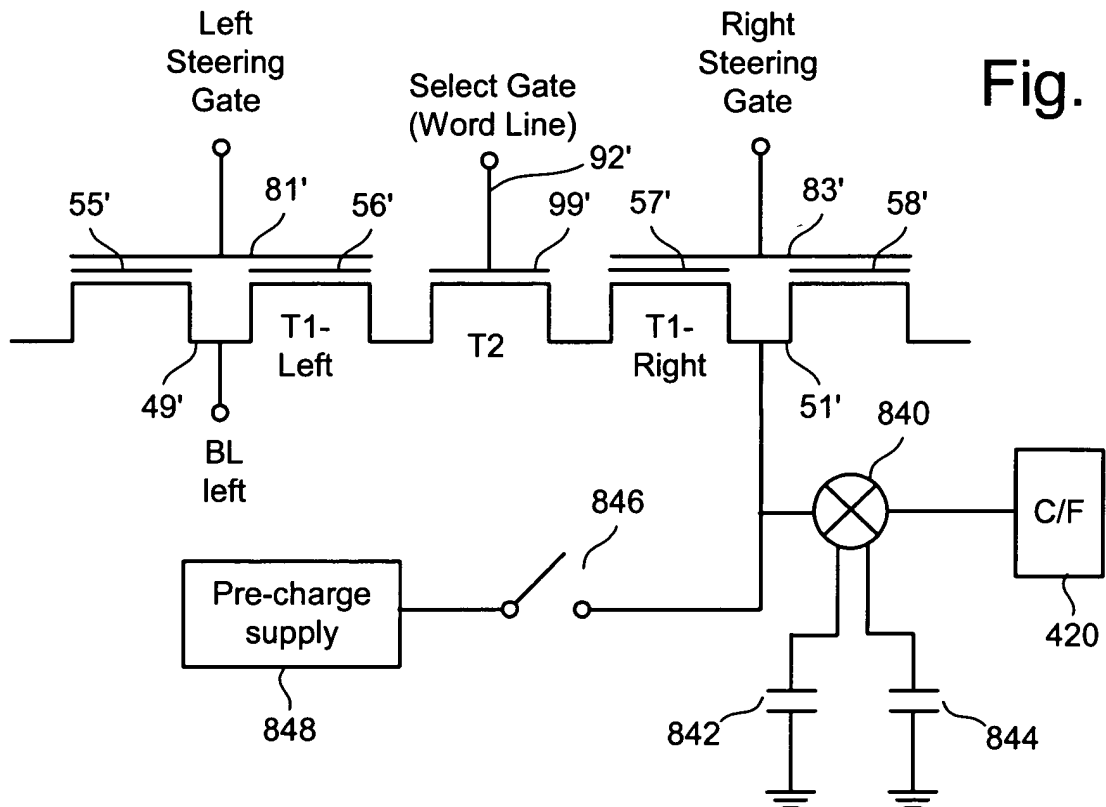


Fig. 25